What is claimed is:

1. An integrated circuit device, comprising:

a bottom layer;

an active chalcogenide layer on the bottom layer;

a top layer on the active chalcogenide layer, wherein the top layer has an rms surface roughness of less than 140Å.

2. The device of claim 1, wherein the top layer has an rms surface roughness of less than about 20Å.

3. The device of claim 1, wherein the top layer has an rms surface roughness of about 10.8Å.

4. The device of claim 1, wherein the top layer is sputtered silver.

5. The device of claim 4, wherein the chalcogenide layer includes diffused silver.

6. An integrated circuit memory cell, comprising:

a first electrode;

a second electrode spaced from the first electrode;

an active chalcogenide layer intermediate the first and second electrodes; and

wherein the second electrode has an outer surface which has an rms surface roughness of less than 140Å.

7. The integrated circuit memory cell of claim 6, wherein the top layer has an rms surface roughness of less than about 20Å.

8. The integrated circuit memory cell of claim 6, wherein the top layer has an rms surface roughness of about 10.8Å.

9. The integrated circuit memory cell of claim 6, wherein the top layer is sputtered silver.

10. The integrated circuit memory cell of claim 9, wherein the chalcogenide layer includes diffused silver.

11. A formative structure for creating chalcogenide integrated circuit devices, comprising:

a bottom layer;

a chalcogenide layer on the bottom layer;

a metal layer on the chalcogenide layer; and

a thin barrier layer on the metal layer, the barrier layer having a thickness such that the barrier layer is essentially transparent to irradiation for diffusing the metal layer into the chalcogenide layer.

12. The structure of claim 11, wherein the thin barrier layer is a thin chalcogenide barrier layer.

13. The structure of claim 12, wherein the thin chalcogenide barrier layer and the chalcogenide layer are formed of a same material.

14. The structure of claim 13, wherein the same material is GeSe.

15. The structure of claim 11, wherein the metal layer includes silver.

16. A chalcogenide memory cell, comprising:

a first electrode;

a chalcogenide layer on the first electrode;

a second electrode on the chalcogenide layer, the top electrode having protrusions thereon with a height of less than 40Å.

17. The chalcogenide memory cell of claim 16, wherein the chalcogenide layer includes a metal diffused therein.

18. The chalcogenide memory cell of claim 17, wherein the second electrode includes a same metal as diffused into the chalcogenide layer.

19. A method of forming a chalcogenide layer in an integrated circuit device, comprising:

forming a first layer;

forming a second layer on the first layer;

forming a third layer on the second layer; and

diffusing the second layer into the first layer to create an integral layer including materials from the first and second layers.

20. The method of claim 19, wherein diffusing to create the integral layer includes irradiating the second layer through the third layer such that the second layer is diffused into the first layer.

21. The method of claim 20, wherein irradiating includes exposing the second layer to ultra-violet light.

22. The method of claim 19, wherein the steps are performed in the recited order.

23. A method of forming a chalcogenide layer in an integrated circuit device, comprising:

forming a first layer;

forming a second layer on the first layer;

forming a third layer on the second layer, wherein the third layer is essentially transparent to irradiation; and

irradiating the second layer through the third layer to cause the second layer to diffuse into the first layer thereby creating an integral layer of materials from the first and second layers.

24. The method of claim 23, wherein forming the third layer includes forming the third layer to a thickness of less then about 30Å.

25. The method of claim 23, wherein forming the third layer includes forming a third layer to a thickness of less than about 50Å.

26. The method of claim 25, wherein forming the third layer includes forming the third layer of a material that is the same as the first layer.

27. The method of 25, wherein forming the first layer includes forming the first layer to have a thickness of about 500 Å and forming the first layer on a substrate.

28. The method of 27, wherein forming the second layer includes forming the second layer to a thickness in a range of about 100 Å to about 200Å.

29. The method of claim 23, wherein forming the third layer includes forming the third layer to have a thickness in the range of about 20Å to about 50Å.

30. A method of forming a doped chalcogenide layer in an integrated circuit device, comprising:

forming a formative chalcogenide layer;

forming a metal layer on the formative chalcogenide layer;

forming a thin barrier layer on the metal layer;

irradiating the metal layer through the thin barrier layer to diffuse the metal layer into the formative chalcogenide layer to create the doped chalcogenide layer.

31. The method of claim 30, wherein irradiating to create the doped chalcogenide layer includes diffusing the metal layer into the thin barrier layer to create a portion of the doped chalcogenide layer that has a smooth upper surface.

32. The method of claim 31, wherein forming the thin barrier layer includes forming the thin barrier layer from a chalcogenide material.

33. The method of claim 32, wherein forming the thin barrier layer includes forming the thin barrier layer from the same chalcogenide material as the formative chalcogenide layer.

34. The method of claim 33, wherein forming the formative chalcogenide layer includes forming the formative chalcogenide layer from GeSe.

35. The method of claim 30, wherein forming the thin barrier layer includes forming the thin barrier layer to a thickness of less than 30Å.

36. The method of claim 30, wherein forming the thin barrier layer includes forming the thin barrier layer to a thickness of less than 50Å.

37. The method of claim 30, wherein forming the thin barrier layer includes forming the thin barrier layer to a thickness in the range of about 20Å to about 50Å.

38. The method of claim 30, wherein forming the metal layer includes forming a silver layer.

39. A method of forming a doped chalcogenide layer in an integrated circuit device, comprising:

forming a formative GeSe layer;

forming a silver layer on the formative GeSe layer;

forming a thin barrier layer on the silver layer;

irradiating the silver layer through the thin barrier layer to diffuse the silver layer into the formative GeSe layer to create the doped chalcogenide layer.

40. The method of claim 39, wherein forming the thin barrier layer includes forming a thin GeSe barrier layer.

41. The method of claim 40, wherein forming the formative GeSe layer includes forming same to a thickness in the range of about 500Å to about 1,000Å, and wherein forming the silver layer includes forming same to a thickness in the range of about 100Å to about 200Å.

42. The method of claim 41, wherein forming the thin GeSe barrier layer includes forming the same to a thickness of less than or equal to about 30Å.

43. The method of claim 41, wherein forming the thin GeSe barrier layer includes forming same to a thickness in a range of about 20Å to about 50Å.

44. A chalcogenide integrated circuit device prepared by a process comprising:

forming a first layer;

forming a second layer on the first layer;

forming a third layer on the second layer; and

diffusing the second layer into the first layer to create an integral layer including materials from the first and second layers.

45. The chalcogenide integrated circuit according to claim 44, wherein diffusing to create the integral layer includes irradiating the second layer through the third layer such that the second layer is diffused into the first layer.

46. The chalcogenide integrated circuit according to claim 45, wherein irradiating includes exposing the second layer to ultra-violet light.

47. The chalcogenide integrated circuit according to claim 44, wherein the steps are performed in the recited order.

48. A chalcogenide integrated circuit device prepared by a process comprising:

forming a first layer;

forming a second layer on the first layer;

forming a third layer on the second layer, wherein the third layer is essentially transparent to irradiation; and

irradiating the second layer through the third layer to cause the second layer to diffuse into the first layer thereby creating an integral layer of materials from the first and second layers.

49. A chalcogenide integrated circuit device prepared by a process comprising:

forming a formative chalcogenide layer;

forming a metal layer on the formative chalcogenide layer;

forming a thin barrier layer on the metal layer;

irradiating the metal layer through the thin barrier layer to diffuse the metal layer into the formative chalcogenide layer to create the doped chalcogenide layer.

50. A chalcogenide integrated circuit device prepared by a process comprising:

forming a formative GeSe layer;

forming a silver layer on the formative GeSe layer;

forming a thin barrier layer on the silver layer;

irradiating the silver layer through the thin barrier layer to diffuse the silver layer into the formative GeSe layer to create the doped chalcogenide layer.

51. A semiconductor die including a chalcogenide integrated circuit device which comprises:

a bottom layer;

an active chalcogenide layer on the bottom layer;

a top layer on the active chalcogenide layer, wherein the top layer has an rms surface roughness of less than 140Å.

52. The semiconductor die of claim 51, wherein the top layer has an rms surface roughness of less than about 20Å.

53. The semiconductor die of claim 51, wherein the top layer has an rms surface roughness of about 10.8Å.

54. The semiconductor die of claim 51, wherein the top layer is sputtered silver.

55. The semiconductor die of claim 54, wherein the chalcogenide layer includes diffused silver.

56. A circuit module comprising a plurality of semiconductor dies, at least one of the semiconductor dies including a chalcogenide integrated circuit device having:

a bottom layer;

an active chalcogenide layer on the bottom layer;

a top layer on the active chalcogenide layer, wherein the top layer has an rms surface roughness of less than 140Å.

57. The circuit module of claim 56, wherein the top layer has an rms surface roughness of less than about 20Å.

58. The circuit module of claim 56, wherein the top layer has an rms surface roughness of about 10.8Å.

59. The circuit module of claim 56, wherein the top layer is sputtered silver.

60. The circuit module of claim 59, wherein the chalcogenide layer includes diffused silver.

61. An electronic system comprising a processor and a memory system, the memory system including a chalcogenide integrated circuit device, which includes:

a bottom layer;

an active chalcogenide layer on the bottom layer;

a top layer on the active chalcogenide layer, wherein the top layer has an rms surface roughness of less than 140Å.

62. The electronic system of claim 61, wherein the top layer has an rms surface roughness of less than about 20Å.

63. The electronic system of claim 61, wherein the top layer has an rms surface roughness of about 10.8Å.

64. The electronic system of claim 61, wherein the top layer is sputtered silver.

65. The electronic system of claim 64, wherein the chalcogenide layer includes diffused silver.

66. Machine executable code stored on machine readable media forming a chalcogenide layer in an integrated circuit device, the machine executable code comprising:

forming a first layer;

forming a second layer on the first layer;

forming a third layer on the second layer; and

diffusing the second layer into the first layer to create an integral layer including materials from the first and second layers.

67. The machine executable code of claim 66, wherein diffusing to create the integral layer includes irradiating the second layer through the third layer such that the second layer is diffused into the first layer.

68. The machine executable code of claim 67, wherein irradiating includes exposing the second layer to ultra-violet light.

69. The machine executable code of claim 66, wherein the steps are performed in the recited order.

70. Machine executable code stored on machine readable media forming a chalcogenide layer in an integrated circuit device, the machine executable code comprising:

forming a first layer;

forming a second layer on the first layer;

forming a third layer on the second layer, wherein the third layer is essentially transparent to irradiation; and

irradiating the second layer through the third layer to cause the second layer to diffuse into the first layer thereby creating an integral layer of materials from the first and second layers.

71. The machine executable code of claim 70, wherein forming the third layer includes forming the third layer to a thickness of less then about 30Å.

72. The machine executable code of claim 71, wherein forming the third layer includes forming a third layer to a thickness of less than about 10Å.

73. The machine executable code of claim 72, wherein forming the third layer includes forming the third layer of a material that is the same as the first layer.

74. The machine executable code of claim 72, wherein forming the first layer includes forming the first layer to have a thickness of about 500 Å and forming the first layer on a substrate.

75. The machine executable code of 74, wherein forming the second layer includes forming the second layer to a thickness in a range of about 100Å to about 200Å.

76. Machine executable code stored on machine readable media forming a chalcogenide layer in an integrated circuit device, the machine executable code comprising:

forming a formative chalcogenide layer;

forming a metal layer on the formative chalcogenide layer;

forming a thin barrier layer on the metal layer;

irradiating the metal layer through the thin barrier layer to diffuse the metal layer into the formative chalcogenide layer to create the doped chalcogenide layer.